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Prioritätsbescheinigung über die Einreichung einer Patentanmeldung

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Bezeichnung:	A method of removing sidewall spacers in the fabrication of a semiconductor device using an improved removal process
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Die angehefteten Stücke sind eine richtige und genaue Wiedergabe der ursprünglichen Unterlagen dieser Patentanmeldung.

München, den 13. März 2003
Deutsches Patent- und Markenamt
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A METHOD OF REMOVING SIDEWALL SPACERS IN THE FABRICATION OF A SEMICONDUCTOR DEVICE USING AN IMPROVED REMOVAL PROCESS

A METHOD OF REMOVING SIDEWALL SPACERS IN THE FABRICATION OF A SEMICONDUCTOR DEVICE USING AN IMPROVED REMOVAL PROCESS

FIELD OF THE PRESENT INVENTION

The present invention relates to the field of fabrication of integrated circuits, and more particularly to a method for improving the etch behavior of sidewall spacers of a semiconductor device.

DESCRIPTION OF THE PRIOR ART

The trend towards an increasing integration density of integrated circuits leads to a further miniaturization of the semiconductor devices of the integrated circuits. The associated shrinkage of device features generates numerous serious challenges for semiconductor manufacturers to provide the devices with the desired electrical characteristics and geometrical structures, also referred to as critical dimensions (CD). Particularly, the formation of the gate electrode with the required shape and with a size in the currently focused sub-100 nm range is rather crucial. In devices having such small feature sizes, the unavoidable diffusion of ions, particularly driven by the required annealing processes during device fabrication, becomes a concern. For example, the lateral diffusion of the ions implanted into the lightly doped drain (LDD) regions, leads to an undesired LDD/gate overlap. The LDD/gate overlap increases the Miller (gate/drain) capacitance, which affects the device switching characteristic and consequently deteriorates the device performance.

The Miller capacitance may be reduced by altering the sequence of the device fabrication process, so that the deep source/drain implantation and annealing are performed prior to the LDD implantation. Thus, the deep source/drain annealing may be carried out without affecting the diffusion of the LDD ions. Implanting the source/drain region prior to the LDD region, however, requires removal of the sidewall spacers employed to define the deep source/drain region, after the deep source/drain implantation process is completed. The sidewall spacers are typically

formed of silicon nitride (SiN) and may be removed by the use of hot phosphoric acid (H_3PO_4). The silicon nitride to silicon etch selectivity of hot phosphoric acid, however, is poor, particularly when the silicon is predoped. The low selectivity causes erosion in undesired regions of the device in the spacer removal process. Thus, controlling of critical dimensions becomes more difficult. The etch selectivity may be improved by forming a thin thermal oxide layer (liner oxide) on the gate electrode of the semiconductor device prior to the formation of the sidewall spacers. Particularly in CMOS devices, however, the spacer removal process is a concern even when a liner oxide is employed.

To explain in detail the use of sidewall spacers, according to a typical prior art process sequence with disposable spacers and a liner oxide, the corresponding process flow for forming an MOS-field effect transistor is described with reference to Figs. 1a-1d.

Fig. 1a schematically depicts a semiconductor device structure 1 comprising a silicon substrate 10, shallow trench isolation regions 20, a gate isolation layer 31 and a gate electrode 41.

A typical process flow for forming the semiconductor structure 1 includes well known lithography, etch and deposition techniques and thus, a description thereof will be omitted.

Fig. 1b depicts the semiconductor device structure 1 after the formation of the sidewall spacers 81 on a liner oxide 85 and during the deep source/drain implantation process 75 resulting in deep source/drain regions 72.

The liner oxide 85 is grown in a thermal oxidation process. Subsequently, the sidewall spacers 81 are formed in an anisotropic etch process, typically in a plasma etch process, from a blanket deposited silicon nitride layer. Subsequently, the implantation process 75 to form the deep source/drain regions 72 is performed, prior to the implantation of LDD regions still to be formed. To activate the implanted ions, a deep source/drain rapid thermal annealing (RTA) process is carried out at a high temperature causing a high diffusivity. Since the LDD regions are not yet

implanted, the deep source/drain region annealing process may not cause an undesired LDD/gate overlap.

The silicon nitride sidewall spacers 81 may be covered with a thin silicon oxide layer (not shown), particularly when the annealing process takes place in an oxygen containing ambient. The thin silicon oxide layer grows in a slow and self-limiting process by conversion of nitride to oxide.

Fig. 1c depicts the semiconductor device structure 1 after the removal of the sidewall spacers 81.

The silicon oxide layer that may cover the sidewall spacers is removed in a hydrogen fluoride (HF) dip process. The silicon nitride sidewall spacers 81 are typically removed by the use of hot phosphoric acid (H_3PO_4). The silicon nitride to silicon oxide etch selectivity of hot phosphoric acid, however, is too low, particularly when the silicon oxide structure is modified by the prior deep source/drain implantation and hence, the liner oxide 85 may not resist the hot phosphoric acid etching in the spacer removal process. Thus, erosion of the thin liner oxide 85 and even erosion of the underlying silicon gate electrode 41 may occur. Such erosion may also occur in the deep source/drain regions 72 where the silicon is heavily doped and consequently, due to the higher etch rate, wherein the etch selectivity is deteriorated. On the other hand, shortening the etch process time may cause an incomplete removal of the silicon nitride sidewall spacers 81. Furthermore, the etch rate of silicon nitride is also affected by the predoping conditions. Thus, the sidewall spacers 81 of n-type and p-type MOSFETs may have a different etch rate in phosphoric acid due to the different dopant concentration.

Fig. 1d depicts the semiconductor device structure 1 after the removal of the liner oxide 85 and during a LDD implantation process 76 for forming LDD regions 71.

The LDD implantation 76 is performed in a known conventional implantation process. The liner oxide 85 may be removed prior to the LDD implantation process 76 by well-known wet-chemical etch processes or may be employed as a screen oxide. The subsequent rapid thermal annealing process, may be advantageously

optimized for the required activation of the LDD regions 71, whereby concurrently the lateral diffusion may be avoided or at least reduced. The diffusivity may be reduced compared to an annealing process required when the deep source/drain regions 72 and the LDD regions 71 have to be annealed in a single process. Thus, lateral diffusion of the LDD ions under the gate electrode 41 (LDD/gate overlap) is reduced and consequently the undesired parasitic capacitances are also decreased and the device performance is improved.

Fig. 1e depicts the semiconductor device structure 1 after the formation of sidewall spacers 82 and silicide regions 91. The newly formed sidewall spacers 82 are required to protect the extension of LDD regions 71 in the subsequent silicide process. The silicide regions 91 are formed in a conventional self aligned silicide process. The silicide process may, for example, be performed by blanket-depositing a layer of refractory metal and by a subsequent two step thermal annealing process, wherein non-reacted excess metal is removed by an appropriate etch process after the first anneal step.

The different etch rates of sidewall spacers of n-type and p-type MOSFETs in phosphoric acid make it more difficult to remove the sidewall spacers in CMOS devices without over-etching and/or leaving spacer residuals. The etch rate of the sidewall spacers depends on the implant parameter of the deep source/drain implantation 75, such as implant species, energies and doses. For p-type transistors typically boron (B) is implanted at an ion energy range of approximately 5 to 45 keV and with a dose of up to approximately $2*10^{15}$ ions/cm^2 is employed. For n-type Transistors typically the heavier arsenic (As) or phosphorus (P) ions having an energy in the same energy range and with a dose of up to approximately $2*10^{15}$-$6*10^{15}$ are used. Thus, the sidewall spacers of n-type transistors show a higher etch rate than the p-type transistors. Failures that may arise from the different dopant concentration and the different doping conditions in the spacer removal process in CMOS devices are illustrated in Figs. 2a to 2c.

Fig. 2a schematically depicts a cross sectional view of a CMOS device structure 2 prior to the removal of sidewall spacers 81. The structure includes an n-type and a p-type field effect transistor, formed on a silicon substrate 10 and separated by

shallow trench isolation regions 20. The transistors comprise a gate insulation layer 31, a gate electrode 41, a liner oxide 85, n-type or p-type deep source/drain regions 72 and the sidewall spacers 81, which may be covered with a thin silicon oxide layer 86.

The field effect transistors are formed as described with respect to Fig 1b for a single transistor, wherein the same reference signs are used to denote similar or identical components or parts.

Fig. 2b schematically depicts the result of an etch process adapted to etch the sidewall spacers 81 of the n-type transistor of the CMOS structure 2. The sidewall spacers 81 of the n-type transistor are substantially completely removed, whereas the removal of the sidewall spacers 81 of the p-type transistor is incomplete and may leave behind residual spacer material 83 that may cause a non-uniform LDD implantation 76 (shown in Fig. 1d).

Fig. 2c contrary thereto depicts the result of an etch process appropriate to etch the sidewall spacers 81 of the p-type transistor of the CMOS structure 2. In this case, the sidewall spacers 81 of the p-type transistor are substantially completely removed, whereas, however, the removal of the sidewall spacers 81 of the n-type transistor may cause undue over-etching, leading to over-etching of the liner oxide 85 and even of the silicon of the gate electrode 41 and of the deep source/drain regions 72.

In view of the problems pointed out above there is a need to adjust the etch rates of sidewall spacers of n-type and/or p-type transistors to enhance uniformity during the removal of spacers of the transistors.

SUMMARY OF THE INVENTION

According to the present invention, a method is provided, wherein disposable sidewall spacers of a semiconductor device are irradiated by ions to modify the structure of the material of the sidewall spacers in order to enhance the etch rate of

the sidewall spacers and to consequently increase the etch selectivity in the corresponding removal process.

According to one illustrative embodiment of the present invention, a method of removing side wall spacers of a semiconductor structure comprises providing a substrate having partially formed semiconductor devices thereon, wherein the devices comprise first and second side wall spacers with a first and second etch rate to a specific etchant, whereby the first etch rate is lower than the second etch rate. The method further comprises implanting ions into the first side wall spacers to adapt the first etch rate to the second etch rate. Furthermore, the method comprises removing the first and second side wall spacers with the specific etchant, whereby a selectivity in removing the first and second sidewall spacers is increased by the implantation of ions.

According to another illustrative embodiment of the present invention, a method of removing side wall spacers of a semiconductor structure comprises providing a substrate having partially formed semiconductor devices thereon, wherein the devices comprise first and second side wall spacers with a first and a second etch rate to a specific etchant, whereby the first etch rate is lower than the second etch rate. The method further comprises implanting ions into the first and second side wall spacers to increase the first and second etch rates, and removing the sidewall spacers with the specific etchant, whereby a selectivity in removing the first and second sidewall spacers is increased by the implantation of ions.

BRIEF DESCRIPTION OF THE DRAWINGS

Further advantages, objects and embodiments of the present invention are defined in the appended claims and will become more apparent with the following detailed description when taken with reference to the accompanying drawings, in which:

Figs. 1a – 1e schematically depict a cross sectional view of a semiconductor device structure, illustrating a typical process flow of the formation of the source/drain regions of a MOS-field effect transistor according to the prior art;

Figs. 2a to 2c schematically depict a cross sectional view of a CMOS device structure illustrating the typical failures occurring in the sidewall spacer removal process in a CMOS-device according to the prior art;

Figs. 3a to 3e schematically depict a cross sectional view of a CMOS device structure illustrating the formation of the source/drain regions of a MOS-field effect transistor in accordance with one illustrative embodiment of the present invention;

Fig. 4 schematically depicts a cross sectional view of a CMOS device structure illustrating a sidewall spacer removal process according to another illustrative embodiment of the present invention; and

Fig. 5 schematically depicts a cross sectional view of a CMOS device structure illustrating the sidewall spacer removal process for a device without a liner oxide according to yet another embodiment of the present invention.

It should be noted that the dimensions shown in the Figures are not true to scale.

DETAILED DESCRIPTION

While the present invention is described with reference to the embodiments as illustrated in the following detailed description as well as in the drawings, it should be understood that the following detailed description as well as the drawings are not intended to limit the present invention to the particular illustrative embodiments disclosed, but rather the described illustrative embodiments merely exemplify the various aspects of the present invention, the scope of which is defined by the appended claims.

The present invention includes the concept of balancing or individually adjusting the etch rates of sidewall spacers of field effect transistors, such as n-type and p-type transistors in CMOS devices, to improve the etch removal process of sidewall spacers. The etch rates may be altered by increasing at least the etch rate of the spacers of the p-type field effect transistor. The etch rate is increased by irradiating ions into the sidewall spacers. Irradiating ions into a solid state feature

changes the structure of the material of the feature into a more amorphous state, i. e. the short range order in the structure of the material is modified. Particularly heavy ions cause strong damage in the solid structure even at a relatively low dose. In one particular embodiment, inert ions are employed so that the electrical characteristics of the implant regions are minimally affected by implanted ions. Thus, the term "inert ions" is to be understood as referring to ions having only a minimal influence on the electrical behavior of the materials employed to form the device features, and substantially not acting as a dopant in the semiconductor regions. Thus, for example, argon (Ar), xenon (Xe), krypton (Kr), and the like may be used as inert ions. For silicon-based or germanium-based device features silicon (Si) or germanium (Ge) ions, respectively, may be considered as "inert ions". On the other hand, implanted semiconductor ions of a different species, for example, germanium ions in a silicon-based device, may alter the device characteristic, and may thus be concurrently employed, for example, for band gap engineering purposes.

With reference to Figs. 3a to 3e, Fig. 4 and Fig. 5, illustrative embodiments according to the present invention will now be described. In Figs. 3a to 3e, Fig. 4 and Fig. 5, the same reference signs as in Fig. 1 and 2 are used to denote similar or equal components and parts.

The embodiments illustrated in Figs. 3a to 3e, Fig. 4 and Fig. 5 relate to a field effect transistor device formed on a silicon substrate 10 and comprising a polysilicon gate device feature 41. The substrate employed, however, is not limited to a silicon substrate, and any other substrate, for example, a germanium substrate or a silicon on insulator (SOI) substrate may be used. Further the employed device is not limited to a field effect transistor and any other feature having a sidewall may be employed. Moreover, the device feature 41 is not limited to a polysilicon gate, and any other gate or interconnect line feature, for example, a metal gate or a polysilicon interconnect line may be used.

The illustrative embodiments according to the present invention shown in Fig. 3a to 3e employ the same steps as described with respect to Figs. 1a to 1e. Thus, Figs.

3a to 3e schematically depict only the additional process steps improving the removal process in a CMOS device.

Fig. 3a depicts a CMOS structure 3, similar to the structure of Fig. 2a, including an n-type and a p-type field effect transistor formed on the silicon substrate 10 and separated by a shallow trench isolation region 20. The transistors comprise n-type or p-type deep source/drain regions 72, and a gate insulation layer 31, the gate electrode 41, a liner oxide 85 and a sidewall spacers 81, respectively.

The transistors may be formed in a process according to a prior art process depicted in Fig. 1b and are n- or p-doped to form the CMOS structure 3. The sidewall spacers 81 may comprise a inorganic material, for example, silicon nitride or may comprise a low-k material, for example, a carbon doped oxide. Low-k materials may reduce parasitic capacitances and may thus increase the device performance and reduce the power consumption of the device.

Fig. 3b depicts the CMOS structure 3 further comprising a mask feature 62.

The mask feature 62 may be formed in a photo-lithographic process, whereby the mask feature 62 may be the resist feature itself or, in other embodiments, a hardmask feature formed by means of depositing a layer of material and performing an etching process to define the hard mask. The mask feature thickness depends on the screening effect of the material and the tilt angle of the implantation and may, for a resist mask, be in the range from approximately 100 to 2000 nm.

Fig. 3c depicts the CMOS structure 3 during a tilted ion implantation process 77.

The dose of the tilted ion implantation process 77 is selected to raise the etch rate of the material of the exposed sidewall spacers 81 of the p-type transistor up to a level that it is substantially equal to the etch rate of the material of the sidewall spacer 81 of the masked n-type transistor.

The sidewall spacers 81 are located at sidewalls extending substantially perpendicular to the surface of the substrate 10. Thus, the sidewall spacers 81 are

typically more extended in that direction. Hence, the implantation is performed with the substrate 10 being tilted to increase the amount of ions irradiated onto the sidewall spacers 81 and to concurrently reduce the undesired irradiation of the adjacent regions of the device. Particularly high tilt angles are appropriate to improve the ratio of ions implanted into the spacers 81 to ions implanted into the adjacent regions of the device. An Implantation at very high tilt angles, however, may suffer from a shielding effect caused by the upper corner of the mask feature 62, since the edge of the mask feature 62 may be located close to the sidewall spacer 81 due to the small distance that n-type and p-type transistors are typically spaced apart in CMOS devices. To compensate the shielding effect, the implantation dose may be increased accordingly to balance the etch rates of the materials of the sidewall spacers 81 of the n-type and p-type transistor. The employed tilt angle for the implantation may range from approximately 10 to 70°.

Fig. 3d depicts the CMOS structure 3 after the removal of the mask feature 62. The mask may be stripped with well known etch methods. Residuals of the resist mask feature 62 may be substantially removed with an resist ash method, wherein the residual resist is oxidized in an oxygen containing plasma. In the cases where a hard mask is employed an etchant appropriate for the selected hardmask material and having the required selectivity to the adjacent device features is used to remove the mask feature 62.

Fig. 3e depicts the CMOS structure 3 after the removal of the sidewall spacers 81.

The thin silicon oxide layer (not shown) that may cover the sidewall spacers 81 is removed in a hydrogen fluoride (HF) dip process according to the prior art, however, the process time is reduced, due to the increased etch rate caused by the ion implantation.

Due to the substantially balanced etch rates the sidewall spacers 81 of the n-type and p-type transistor may be removed in a common etch step, thereby leaving less residuals of spacer materials and causing less etching of the liner oxide 85.

In another embodiment depicted in Fig. 4 the CMOS structure 4 of Fig. 3a is irradiated with ions without forming the mask feature 62. Thus, the mask feature 62 may not shield the ion radiation and a higher tilt angle of the substrate in the range from approximately 10 to 85° may be employed. Therefore the ratio of ions implanted into the sidewall spacers 81 to ions implanted into the adjacent regions of the CMOS device is increased. Due to the increased ratio, the dose of ions irradiated on the substrate 10 may be increased without unduly affecting the characteristic of the CMOS device. Thus, mainly the etch rate of the sidewall spacers 81 is increased and hence, the etch selectivity is improved. Concurrently, the high doses implantation into both the sidewall spacers 81 of the n-type and p-type transistors may reduce the etch rate differences of the materials of the sidewall spacers 81 of both transistor types. Thus, the sidewall spacers 81 of the n-type and p-type transistor may also be removed in a common etch step, thereby leaving less residuals and causing less etching of the liner oxide 85.

Fig 5 depicts yet another embodiment, wherein the liner oxide 85 may be omitted due to the improved etch selectivity and the increased etch rate. Although the etch selectivity of silicon nitride to silicon of hot phosphoric acid is lower than that of silicon nitride to silicon oxide it may be sufficient to remove the sidewall spacers 81 without unduly affecting the adjacent silicon even in the predoped regions such as the gate electrode 41 and the deep source/drain regions 72.

Further modifications and variations of the present invention will be apparent to those skilled in the art in view of this description. Accordingly, the description is to be construed as illustrative only and is for the purpose of teaching those skilled in the art the general manner of carrying out the present invention. It is to be understood that the forms of the invention shown and described herein are to be taken as the presently preferred embodiments. It should be further noted that the embodiments described above may be combined with each other in any appropriate manner.

CLAIMS

1. A method of removing side wall spacers of a semiconductor structure, the method comprising:

   providing a substrate having partially formed semiconductor devices thereon the devices comprising first and second side wall spacers with a first and a second etch rates with respect to a specific etchant, whereby the first etch rate is lower than the second etch rate;

   implanting ions into the first side wall spacers to adapt the first etch rate to the second etch rate; and

   removing the first and second sidewall spacers with the specific etchant, whereby a selectivity in removing the first and second sidewall spacers is increased by the implanting of said ions.

2. The method of claim 1, wherein the partially formed semiconductor devices are partially formed n-type and p-type field effect transistors.

3. The method of claim 1, wherein the semiconductor structure is a CMOS structure.

4. The method of claim 1, wherein a mask covering at least the second side wall spacers is employed to implant the ions into the first side wall spacers.

5. The method of claim 4, wherein the mask is formed by photolithography.

6. The method of claim 4, wherein the mask is one of a photo resist mask and a hard mask.

7. The method of claim 6, wherein the photo resist mask has a thickness of 100 to 2000 nm

8. The method of claim 1, wherein the ions are substantially inert ions.

9. The method of claim 1, wherein the ions are at least one of argon ions, xenon ions, germanium ions and silicon ions.

10. The method of claim 1, wherein the ion implant dose is in the range from approximately $1*10^{13}$ to $1*10^{15}$ ions/cm^2

11. The method of claim 1, wherein the ion energy is in the range from approximately 10 to 80 keV.

12. The method of claim 1, wherein a tilt angle between a surface of said substrate and a direction of incidence of the ions is in the range from 10 to 70°.

13. The method of claim 1, wherein the material of the side wall spacers comprises an inorganic material.

14. The method of claim 1, wherein the material of the side wall spacers comprises a low-k material.

15. The method of claim 1, wherein the material of the side wall spacers is silicon nitride.

16. The method of claim 1, wherein prior to the step of implanting ions into said side wall spacers, dopants are implanted into the side wall spacers during the formation of a source and a drain region in the partially formed semiconductor device.

17. The method of claim 16, wherein the dopants are at least one of boron, arsenic and phosphorous.

18. The method of claim 1, wherein the partially formed semiconductor devices comprises a gate feature and the measure of the gate feature in one direction is 100 nm or less.

19. A method of removing side wall spacers of a semiconductor structure, the method comprising:

providing a substrate having partially formed semiconductor devices thereon, the devices comprising first and second side wall spacers with a first and a second etch rate to a specific etchant, whereby the first etch rate is lower than the second etch rates;

implanting ions into the first and second side wall spacers to increase the first and second etch rate;

removing the first and second sidewall spacers with the specific etchant, whereby a selectivity in removing the first and second sidewall spacers is increased by the implanting of ions.

20. The method of claim 19, wherein the partially formed semiconductor devices are partially formed n-type and p-type field effect transistors.

21. The method of claim 19, wherein the semiconductor structure is a CMOS structure.

22. The method of claim 19, wherein the ions are substantially inert ions.

23. The method of claim 19, wherein the ions are at least one of argon ions, xenon ions, germanium ions and silicon ions.

24. The method of claim 19, wherein the ion dose is in the range from approximately $1*10^{14}$ to $1*10^{15}$ ions/cm^2

25. The method of claim 19, wherein the ion energy is in the range from approximately 10 to 80 keV.

26. The method of claim 19, wherein a tilt angle between a surface of the substrate and a direction of incidence of the ions is in the range from approximately 10 to 85°.

27. The method of claim 19, wherein the material of the side wall spacers comprises an inorganic material.

28. The method of claim 19, wherein the material of the side wall spacers comprises a low-k material.

29. The method of claim 19, wherein the material of the side wall spacers comprises silicon nitride.

30. The method of claim 19, wherein prior to said implanting of ions dopants are implanted into the side wall spacers during the formation of a source and a drain region.

31. The method of claim 30, wherein the dopants are at least one of boron, arsenic and phosphorous.

32. The method of claim 19, wherein the partially formed semiconductor device comprises a gate feature and a dimension of the gate feature in at least one direction is 100 nm or less.

ABSTRACT

A method for improving the etch behavior of sidewall spacers in the fabrication of a CMOS device is disclosed. The etch rate of the material of the sidewall spacers depends on the implantation conditions. Thus, the etch rates are different for n-type and p-type transistors. To remove the sidewall spacers properly, the etch rates are altered by an implantation of ions, thereby modifying the structure of the material of the sidewall spacers and increasing the etch rate of the material. The increased etch rate leads to a shorter process time in the spacer removal process. Thus, the surrounding regions are less affected by the removal process and the device reliability and performance is improved.

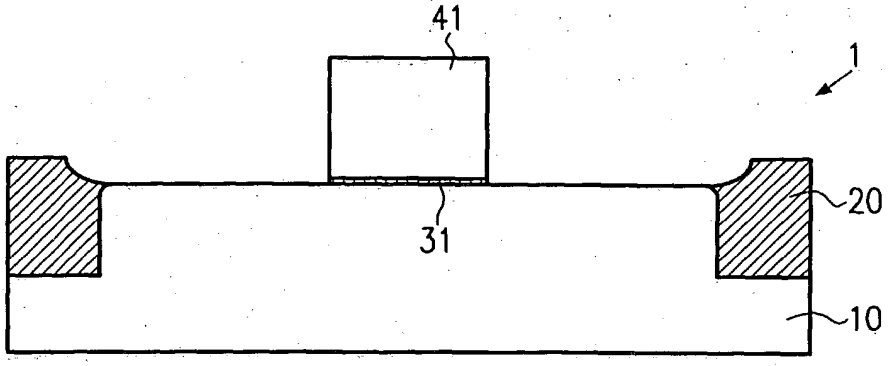

FIG.1a
(prior art)

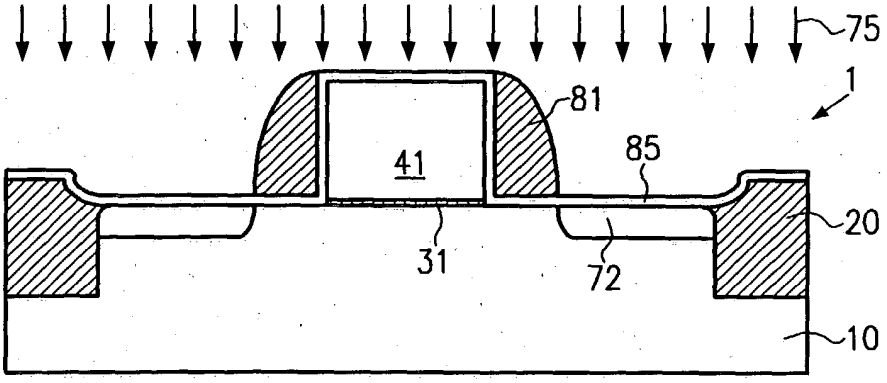

FIG.1b
(prior art)

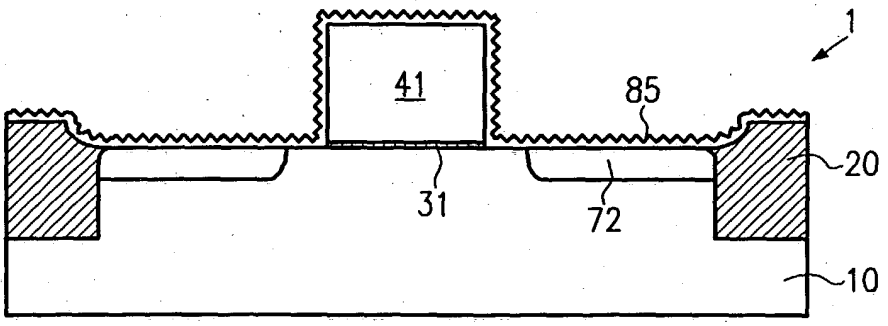

FIG.1c
(prior art)

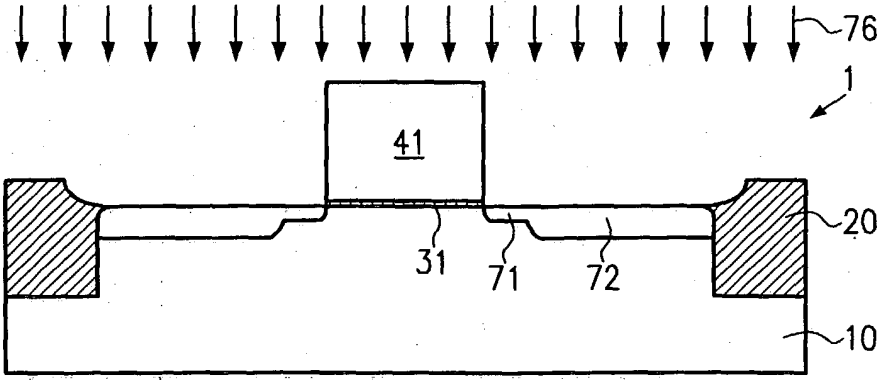

FIG.1d
(prior art)

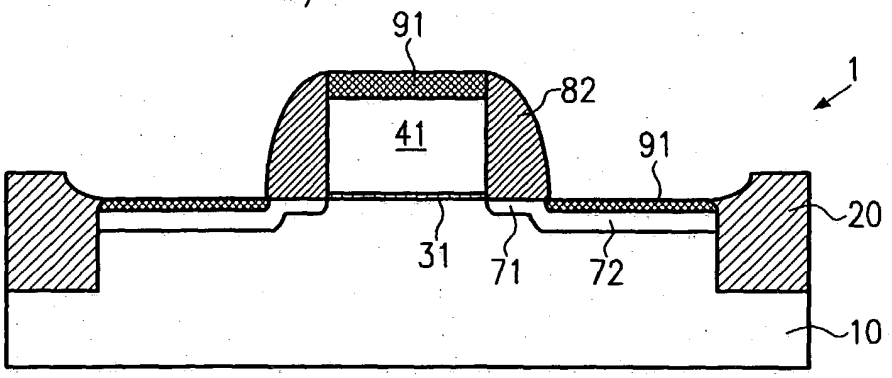

FIG.1e
(prior art)

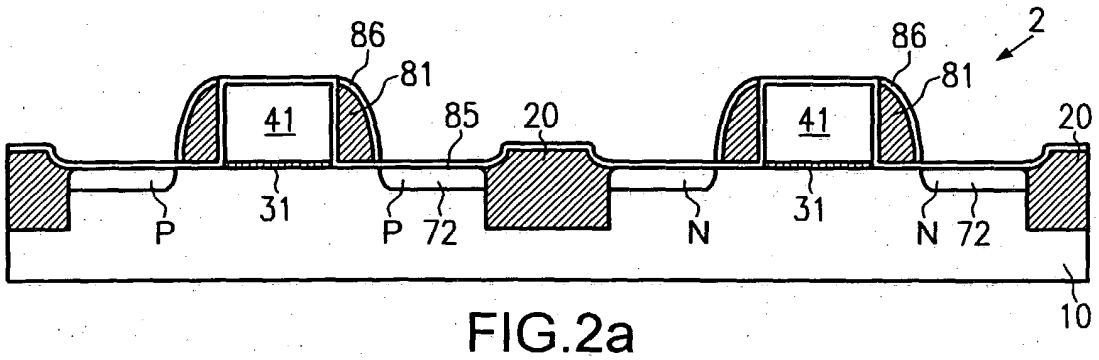

FIG.2a
(prior art)

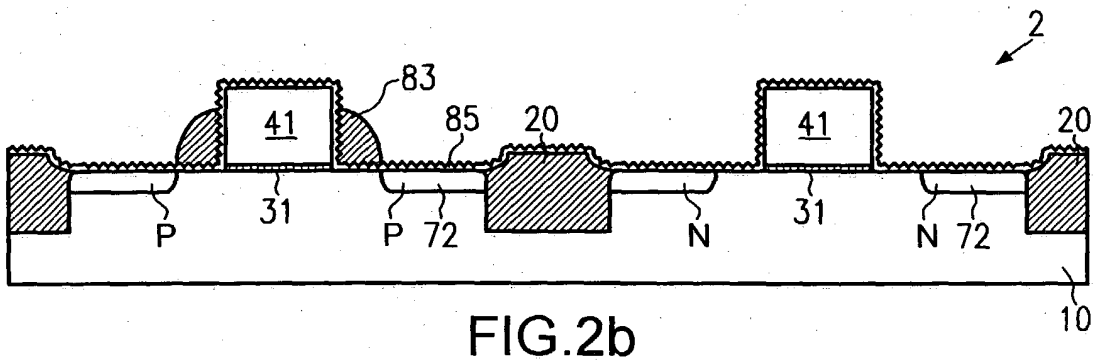

FIG.2b
(prior art)

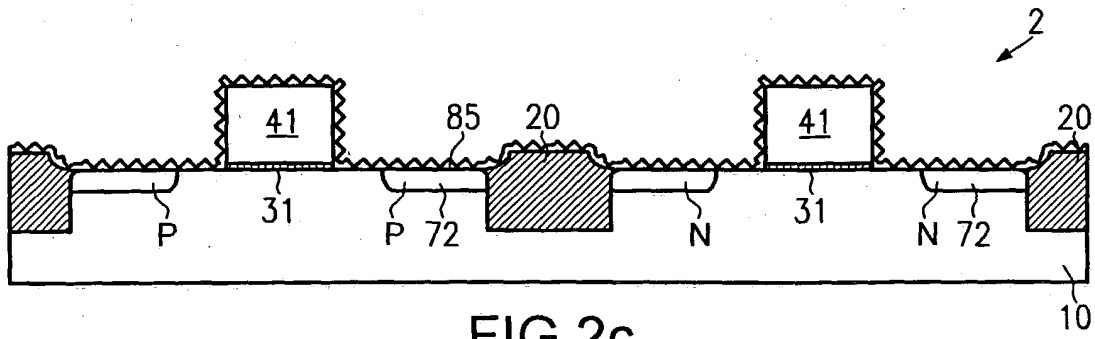

FIG.2c
(prior art)

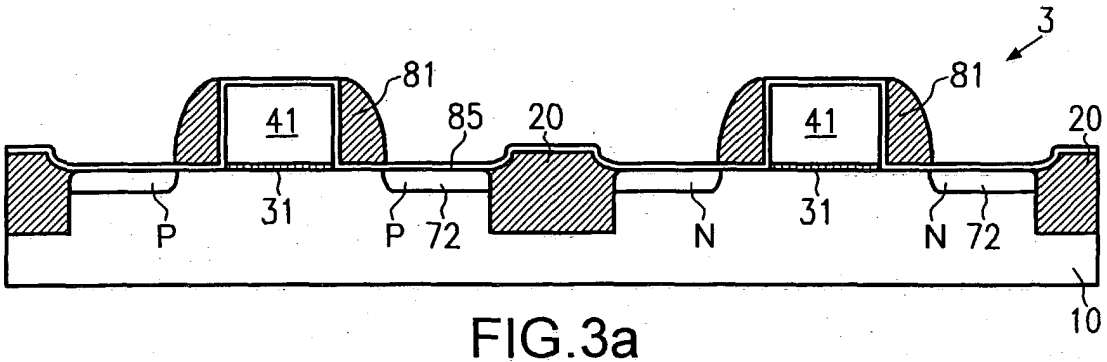

FIG.3a

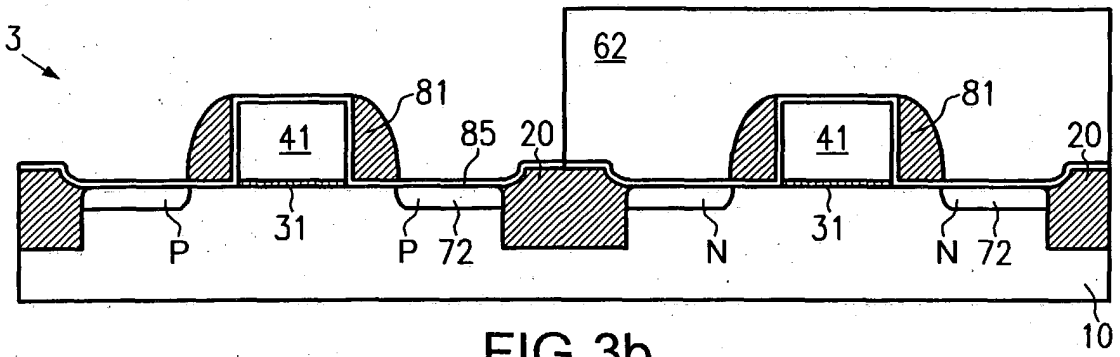

FIG.3b

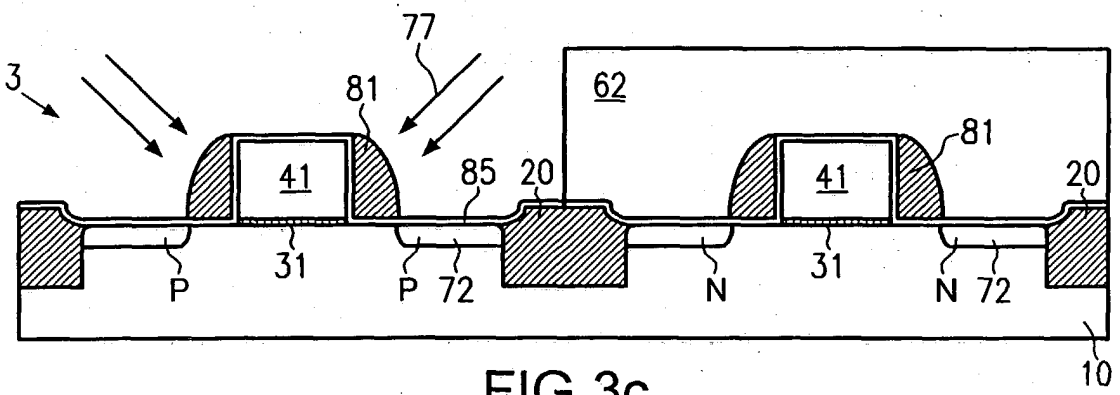

FIG.3c

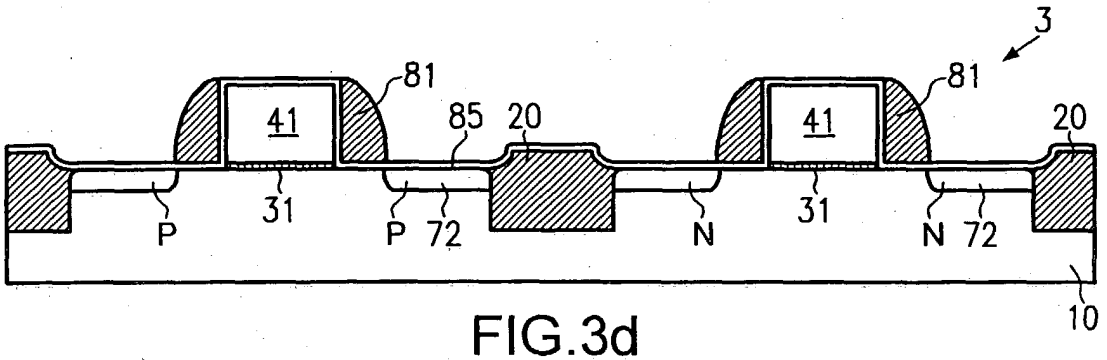

FIG.3d

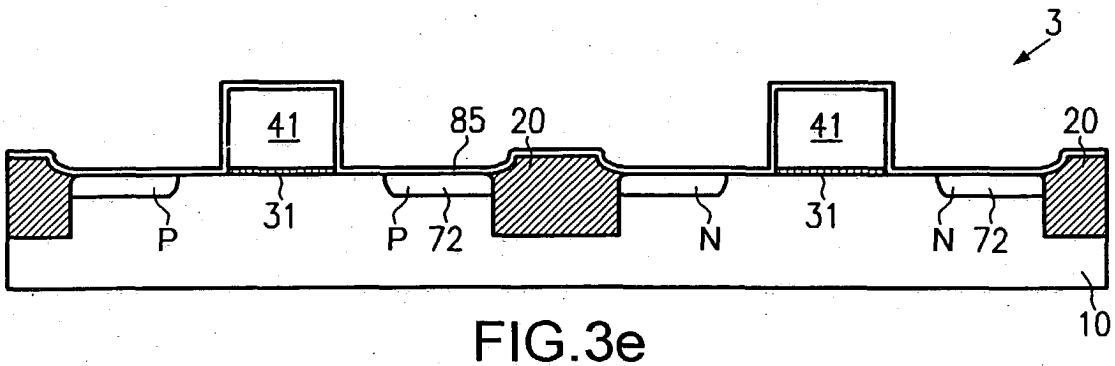

FIG.3e

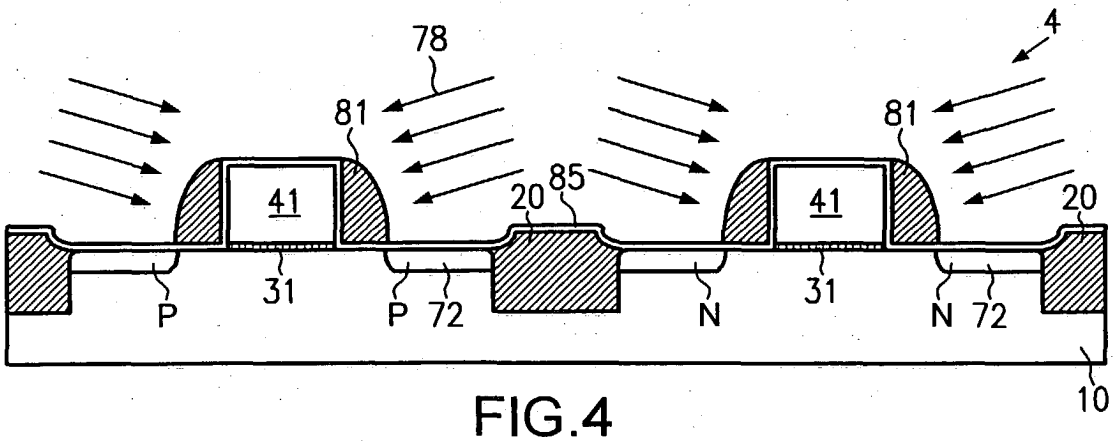

FIG.4

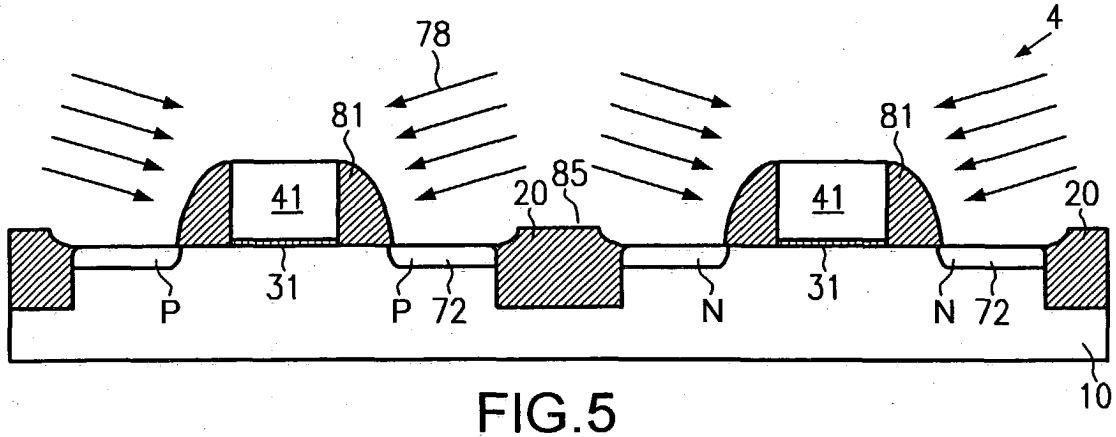

FIG.5